Computing Worst-Case Contention Delays for Networks on Chip

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I. Extended Abstract

A. Introduction

Computing performance needs in domains such as automotive, avionics, railway, and space are on the rise. This is fueled by the trend towards implementing an increasing number of product functionalities in software that ends up managing huge amounts of data and implementing complex artificial-intelligence functionalities [1], [2].

Manycores are able to satisfy, in a cost-efficient manner, the computing needs of embedded real-time industry [3], [4]. In this line, building as much as possible on manycore solutions deployed in the high-performance (mainstream) market [5], [6], contributes to further reduce costs and increase availability. However, commercial off the shelf (COTS) manycores bring several challenges for their adoption in the critical embedded market. One of those is deriving timing bounds to tasks' execution times as part of the overall timing validation and verification processes [7]. In particular, the network-on-chip (NoC) has been shown to be the main resource in which contention arises, and hence hampers deriving tight bounds to the timing of tasks [8].

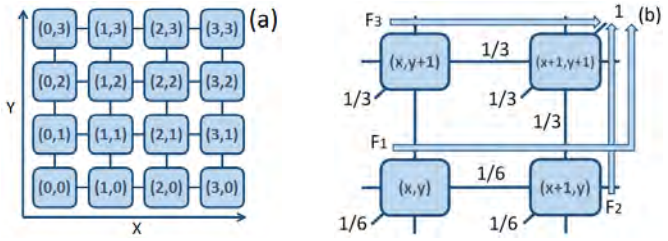
For widely-used wormhole NoCs (wNoCs) [6], [5], several proposals show how to compute latency upperbounds to the different flows communicating on the manycore [9], [10] under some restrictions, e.g. deterministic routing. Unfortunately, WCET estimates computed with wNoCs are generally pessimistic when – as required to achieve composable estimates – no restrictions are imposed on when and where interference occurs in the wNoC. Interestingly, wNoCs offer several software-controllable parameters that allow to optimize (reduce) the worst-case contention delay (WCD) that packets crossing can suffer. These include mapping, routing, and allocation of weights (referred to as walloc) to arbitration policies in each router. NoC contention optimization solutions have been proposed for mapping [11], [12] and combining routing and mapping [13], [14]. Additionally, optimal allocation of weights to achieve fair bandwidth balancing have been also proposed for TDMA [15] and wNoCs [16]. In general, those solutions do not tackle all parameters at once, which leads to globally suboptimal solutions.

Overall, reducing the WCD in NoCs is indeed a multidimensional problem and, to make things worse, strong dependencies exist between the different parameters. For instance, the impact of routing in WCD is heavily affected by the mapping of tasks to cores.

Despite the inter-dependences among these parameters, to our knowledge, no previous work proposes an integral solution to the problem of WCD reduction simultaneously optimizing mapping, routing and walloc.

B. Contribution

In this study, we cover this gap by proposing a wNoC ILP- and stochastic-based optimization framework that minimizes WCD estimates (and hence WCET estimates) of applications running in the wNoC-connected manycores.



(a) 2D Mesh router coordinates

(b) Unfair round-robin bandwidth allocation under wormhole switching

Fig. 1: Mesh manycore system and how mapping, routing and bandwidth allocation parameters have impact in the WCD

We focus the target of this study in systems build with 2D mesh NoC topologies like the ones showed in Figure 1, even though the same analysis can be done to other topologies. In Figure1(a), we show a block diagram of a 2D mesh multicore system where each node coordinate represents a router that has attached a processor and/or a memory element and it is connected to the other routers forming a mesh topology.

Our target is to create a framework that given some tasks that are going to run on the top of a mesh multicore system, it optimizes the mapping, routing and bandwidth allocation configuration of the mesh all at the same time so as to reduce the WCET estimates of these tasks. One of the possible NoC configuration outputs after running the optimizing framework is shown in Figure 1(b). In this figure, we show a feasible NoC solution for the three main NoC parameters object of these study: mapping assigned as first come first serve (FCFS), XY routing algorithm and round-robin bandwidth arbitration).

In this study:

1) We analyze the main wNoC parameters that cause variability in WCD (mapping, routing, and walloc) separately and how they relate to each other. We propose a particular WCD-centric abstraction to address the main sources of jitter in a wNoC, namely: placement of tasks (threads) to cores, routing, and weighted bandwidth allocation (walloc).
2) We show that reducing WCD is a multidimensional problem that we decompose into a stochastic-based optimization and an ILP formulation. The former covers the optimization of the routing, whereas the latter optimizes mapping and walloc.
3) We compare the effectiveness of the ILP method with respect to hand-made setups and other approaches that optimize a subset of the parameters. Our results confirm that our multidimensional optimization approach achieves performance guarantees that outperform the other ones evaluated. We also show that optimizing virtual-channel (VC) allocation provides a subset of the configurations obtained with walloc, so that optimizing walloc makes VC not to provide any additional advantage.

We focus on high-performance wormhole NoCs in which time-predictability is achieved by leveraging an optimal configuration of parameters. This includes features like arbitration and routing already configurable from software in existing real wNoC designs. Weight allocation, while to our knowledge it has not been implemented in commercial NoCs yet, it is widely used in high-performance routers for off-chip wormhole networks [17]. Given that the implementation cost of weighted arbitration is quite low [16], they can be included with low cost in high-performance on-chip designs. Moreover, modifications required to implement weighted arbitration are local in contrast to hardware proposals that require global changes like, new signals among routers and nodes, different flow-control, global clocks or the like.

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Jordi Cardona is a PhD. Student for the CAOS group at BSC. He obtained his M.S. degree in 2018 and graduated in Informatics Engineering in 2016, both titles obtained from the Universitat Politcnica de Catalunya. He enrolled BSC in 2016 where he started working on the analysis of COTS networks on chip for real-time multicore systems during his master thesis and his current research focuses on monitor and control contention in shared resources of critical real-time systems.